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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,160	03/17/2005	Ichiro Hazeyama	Q86110	6481

23373 7590 11/02/2006

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
TAYLOR, EARL N	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/528,160	HAZEYAMA ET AL.	
	Examiner	Art Unit	
	Earl N. Taylor	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,6 and 7* is/are allowed.

6)☒ Claim(s) *1,5,8 and 13* is/are rejected.

7)☒ Claim(s) *2,3 and 9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to Claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

Figures 22-29 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masami (JP Pat. 08-340021) in view of Gilleo et al. (THERMOPLASTIC ADHESIVES – THE ATTACHMENT SOLUTION FOR MULTICHIP MODULES) or Furutani et al. (U.S. Patent 5,668,247).

Referring to Claim 1, Masami discloses, in Fig. 1, a semiconductor package comprising: a semiconductor device (2) with one or more device-side electrodes (4) being formed on a circuit-bearing surface; and a flexible substrate having a patterned wiring (32) and a polyimide layer which functions as a insulating layer (30, 31) formed on either or both sides of the patterned wiring (32) (par. 45 and 46), the flexible substrate being bent around said semiconductor device (2), wherein: said flexible substrate has a first electrode (17) provided on said semiconductor device-side surface of said flexible substrate, the first electrode (17) being connected to said device-side electrode (4) of said semiconductor device and sealed by said insulating layer (30, 31), and a second electrode (21, 23) provided on a surface different from the surface on which said first electrode (17) is provided; and said flexible substrate has at least two or more layers of patterned wiring formed thereon (Fig. 1; abstract; par. 58 and 59) but does not specifically teach wherein the insulating layer is specifically a thermoplastic adhesive. Gilleo teaches packaging applications with the use of thermoplastic adhesives to adhere the semiconductor die to a wiring substrate (*Applications* section). Therefore it would have been obvious to one of ordinary skill in the art to use a thermoplastic adhesive as taught by Gilleo as the insulating layer of Masami thereby removing the need for separate adhesives, allowing for ease in re-workability because

of the thermoplastic adhesive's fixed softening point and predictable temperature viscosity (*Rework* section) and ease of manufacturing semiconductor devices due to the thermoplastic adhesive's properties of softening or melting when heated and returning to a solid when cooled (*Polymer Basics* section). Furutani teaches a thermoplastic polyimide adhesive to laminate conductive wiring. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the thermoplastic polyimide adhesive layer taught by Furutani for the polyimide layers taught by Masami thereby removing the need for separate adhesives and that produces desirable properties at low temperatures and also protects the wiring from unwanted degradation during a thermal fusion process (abstract; Col. 1, Lines 7-33 and Col. 2, Lines 40-50).

Referring to Claim 5, Masami in view of Gilleo or Furutani teach all of the limitations of Claim 1, wherein said flexible substrate has a cavity formed on said flexible substrate so as to accommodate said semiconductor device (2) in said cavity portion. The flexible substrate that surrounds the semiconductor device forms a cavity that accommodates the semiconductor device.

Referring to Claim 8, Masami in view of Gilleo or Furutani teach all of the limitations of Claims 1 and 5 wherein a plurality of semiconductor packages form stacked semiconductor package and are electrically connected via said electrodes and three-dimensionally stacked in layers (see Drawings 8, 9 and 12-17).

Referring to Claim 13, Masami in view of Gilleo or Furutani teach all of the limitations of Claim 1 wherein the substrate is adhered to the sides of the chip as shown.

Allowable Subject Matter

Claims 4, 6 and 7 are allowed.

Claims 2, 3 and 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 2, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein said flexible substrate has a portion which is thinner or has a smaller number of wiring layers formed at a bend of said flexible substrate or on a region including the bend than at another portion of the flexible substrate in combination with all of the limitations of Claims 1 and 2. Claims 3, 9 and 10 include all of the limitations of Claim 2.

Regarding Claim 11, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein the cavity is formed by a portion of the flexible substrate having a smaller number of wiring layers than another portion of the flexible substrate in combination with all of the limitations of Claims 1, 5 and 11.

Regarding Claim 12, the prior art of record alone or in combination neither teaches nor makes obvious the invention wherein the cavity is formed by a portion of the flexible substrate being thinner than another portion of the flexible substrate in combination with all of the limitations of Claim 1, 5 and 12.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

Andy Huynh
Primary Examiner